UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,762	11/15/2002	Wei-Pin Chen	JCLA8424	9203

23900 7590 01/07/2009

J C PATENTS, INC.
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER	
NICKERSON, JEFFREY L	
ART UNIT	PAPER NUMBER
2442	
MAIL DATE	DELIVERY MODE
01/07/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/065,762	CHEN ET AL.	
	Examiner	Art Unit	
	JEFFREY NICKERSON	2442	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Application No. 10/065,762 filed on 15 November 2002. The request for continued examination presented on 16 October 2008, which cancels claims 14-20, and provides change to claims 1-4 and 9, is hereby acknowledged. Claims 1-13 have been examined.

Claim Objections

2. Claims 1-8 are objected to under 37 CFR 1.75(d)(1) because of an improper use of antecedent basis.

Regarding claim 1, this claim recites the limitation "the message target row" in the second-to-last line. There is insufficient antecedent basis for this limitation in the claim, and it should be changed to "the target message row." Correction is required.

Regarding claim 2, this claim recited the limitation "the message target row" in lines 6 and 7. There is insufficient antecedent basis for this limitation in the claim, and it should be changed to "the target message row." Correction is required.

Regarding claims 3-7, these claims inherit the informality of their parent claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 1 and 9, applicant adds the following limitation to claim 9 (claim 1 contains similar content):

> *"clearing the distribution flag and write complete flag of the target message row without permission of the source controller".*

Applicant asserts the concept of "clearing a flag without permission" is inherently supported in paragraphs [0006], [0017], and Fig. 1, which state that "*the distribution complete flag and the write complete flag of the message row are cleared by the read pointer control unit, rather than the write control unit or source controller*". The examiner respectfully disagrees with applicant's assertion. Nowhere in the cited support sections does it describe permission requirements or lack thereof for clearing shared flags.

Furthermore, the phrase "without permission" is ambiguous and could take several different meanings (See 2nd paragraph rejection below). If it means, "receives no indication from the source controller that the destination controller can access the resource and subsequently clear the flag", then, in fact, applicant's invention does have a permission indication scheme in place. Paragraph [0006] and [0017] indicates that the source controller indicates to the destination controller when it should have access to the message row by setting the write complete flag, and thus giving the destination controller permission to access to the shared message row and control flags. The destination controller returns resource access permission to the source controller by clearing the flag.

Regarding claims 2-8 and 10-13, these claims inherit the non-enabled features of their parent claims.

6. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1 and 9, applicant claims the concept of "clearing a flag without permission from a controller". It is unclear what requirements the phrase "without permission" imposes upon the system. For instance, it could mean that the flag clearer receives no direct permission indication (i.e. a handshaking signal) from the controller

prior to accessing the shared resource and clearing the flag. Or, it could mean that the flag clearer receives no indirect or implicit permission indication from the controller prior to accessing the shared resource and clearing the flag. However, every system with a shared resource has some type of access regulation scheme, whether it provides permission indirectly (for instance, by throwing a flag), provides permission implicitly (for instance, via a strict timing sequence such as timeslots), or provides permission directly (via the controller sending a signal to the flag clearer to access the shared resource and flag). If the flag was a non-shared resource, then the de facto standard would be to clear the flag without permission, because if I am the sole owner and manipulator of a flag then I would never ask permission to use it. The wording of the claim, however, makes it seem as if the flag clearer "doesn't receive an indication of permission after reading the shared resource and prior to clearing the shared flag". If this is the definition for "without permission", then every system with single owner shared resource locks does this. A resource owner does not clear their lock flag until after they've completed using the resource (if that is a read as claimed), and since they are the resource owner, they don't need permission from anyone else to manipulate the resource lock. Therefore, one of ordinary skill in the art at the time of the invention would not recognize the phrase "without permission" as being clear and definite, in regard to a shared resource.

Regarding claims 2-8 and 10-13, these claims inherit the indefiniteness of their parent claims.

Response to Arguments

7. Applicant's arguments filed 16 October 2008 have been fully considered but they are not persuasive.

Independent claims 1 and 9

Applicant argues several limitations are not taught by the combined teachings of Kawauchi (US 5,619,653), Nanba (US 4,665,484) and Fujimoto (US 5,418,913). Specifically, applicant argues the combined teachings do not teach the following limitation:

"the distribution complete flag and the write complete flag of the message target row are both cleared without permission of the write control unit and the source controller".

The examiner respectfully disagrees. Nanba teaches the use of a test and set instruction, which, after a owner has gained control and locked the shared resource, the owner can clear the lock flag without permission from any other controller (Nanba: col 1, lines 17 - col 2, line 41).

Applicant argues that it would not be obvious to combine Nanba with Kawauchi because it would change the principle purpose of Nanba, and render Nanba unsatisfactory for its intended purpose.

The examiner respectfully disagrees. Nanba's teachings were introduced solely for the teachings and explanation of a test and set operation, the utilization of which would be obvious to one of ordinary skill in the art in the handling of a shared resource.

Applicant's arguments are ultimately unpersuasive and, therefore, the rejections of these claims are hereby maintained.

Dependent claims 2-8 and 10-13

Applicant argues these claims conditionally on the arguments of their parent independent claims.

Applicant's arguments are ultimately unpersuasive and, therefore, the rejections of these claims are hereby maintained.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3, 7-9, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), and further in view of Nanba (US 4,665,484) and Fujimoto (US 5,418,913).

Regarding claim 1, Kawauchi teaches a buffer device (Kawauchi: abstract specifies a data buffer device), for transmitting a plurality of messages between a source and destination, comprising:

a plurality of messages rows (Kawauchi: Figure 3 depicts multiple data columns), for storing the messages that the source intends to transmit to the destination (Kawauchi: abstract), each of the message rows at least comprising a write complete flag (Kawauchi: abstract specifies write attribute flags);

a write control unit (Kawauchi: Figure 3, item 110 depicts the buffer controller), coupled to the source and the plurality of message rows (Kawauchi: Figure 3, see also col 4, lines 3-17), used to sequentially output a plurality of free message row addresses (Kawauchi: Figure 3; col 4, lines 3-17 specifies that the write pointer sequentially acquires buffer addresses), wherein when the message transmitting queue still has a free message row, the source controller reads an address of a target message row that is currently free among said plurality of message rows (Kawauchi: Figure 3; col 4, lines 3-17; col 4, lines 45-58 specifies it does not use addresses if they've already been written to), and when the source completes writing a message of the target message row, the write complete flag of the target message row is set (Kawauchi: Figure 3, col 4,

lines 3-17; col 4, lines 45-58 specifies the write attribute bit is flagged once writing is complete), and when the message transmitting queue has no free message row, said write control unit outputs a non-free message row signal (Kawauchi: Figure 3, item 100; col 3, lines 31-57 specify there is a "reception ready" signal for the buffer device, equivalent to a NOT "not free address" signal and used for the same purpose);

and a read control unit (Kawauchi: Figure 3, item 110 depicts the buffer controller), coupled to the destination and the plurality of message rows (Kawauchi: Figure 3; see also col 3, lines 23-57), to read the message of the target message row when the write complete flag of the target message row is set, wherein once the destination completes reading the message of the target message row, the write complete flag of the target message row is cleared (Kawauchi: col 5, lines 22-35).

Kawauchi does not teach the use of a distribution complete flag, wherein the distribution complete flag is set when the shared resource has began to be used, and wherein the distribution complete flag is cleared after the use of the shared resource and cleared without permission of the write control unit and the source controller; or

issuing a read request for informing the destination to read the shared data and subsequently reading the data in response to the read request.

Nanba, in a similar field of endeavor, the use of a distribution complete flag, wherein the distribution complete flag is set when the shared resource has began to be used, and wherein the distribution complete flag is cleared after the use of the shared resource and cleared without permission of the write control unit and the source

controller (Nanba: col 1, lines 17 – col 2, line 41 specifies a test and set instruction, which uses a lock control flag on shared memory).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Nanba for using a test and set instruction. The teachings of Nanba, when implemented in the Kawauchi system, will allow one of ordinary skill in the art to handle multithreaded accesses to shared memory. One of ordinary skill in the art would be motivated to utilize the teachings of Nanba in the Kawauchi system in order to prevent race conditions during accessing of shared memory by multiple threads.

The Kawauchi/Nanba system does not teach issuing a read request for informing the destination to read the shared data and subsequently reading the data in response to the read request.

Fujimoto, in a similar field of endeavor, teaches issuing a read request for informing the destination to read the shared data and subsequently reading the data in response to the read request (Fujimoto: Figure 4, "Receiver's Identity" rows; Figure 6, item 110; col 13, lines 22-46 specifies an interrupt is sent to the processor associated with the queue so it can start reading).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Fujimoto for sending interrupts to receiving processors identifying that data is ready to be read. The teachings of Fujimoto, when implemented in the Kawauchi/Nanba system, will allow one of ordinary

skill in the art to utilize organized reading from destination controllers by using interrupts. One of ordinary skill in the art would be motivated to utilize the teachings of Fujimoto in the Kawauchi/Nanba system in order to allow efficient and quick reading of a queue from multiple processors by using interrupts.

Regarding claim 3, the Kawauchi/Nanba/Fujimoto system teaches wherein the read control unit comprises:

a read pointer control unit, to store a read address of the message transmitting queue (Kawauchi: Figure 3, item 103), wherein when the destination controller completes reading the message of the message row pointed to by the read address, said read pointer control unit clears the distribution complete flag and the write complete flag of the message row pointed to by the read address (Kawauchi: Figure 3, items 102 and 103; col 5, lines 22-35; Nanba: col 1, lines 17-45), and progresses the read address (Kawauchi: abstract specifies reading is sequential);

a read buffer, coupled to the read pointer control unit and the plurality of message rows, to temporarily store the message of the message row pointed to by the read address (Fujimoto: Figure 10, items 115 provides the receiving processor is storing the message);

and a read request multiplexer, coupled to the read pointer control unit and the write complete flags of the plurality of message rows, to output the read request according to the write complete flag of the message row pointed to by the read address

(Fujimoto: col 1, line 50 – col 2, line 6 specifies that obtaining read pointer address from flag status in a queue is well known in the art).

Regarding claim 7, the Kawauchi/Nanba/Fujimoto system teaches wherein the source is a central processing unit (Fujimoto: Figure 1a, item 1 and Figure 9, items 114).

Regarding claim 8, the Kawauchi/Nanba/Fujimoto system teaches wherein the destination is a central processing unit (Fujimoto: Figure 1a, item 2 and Figure 9, items 114).

Regarding claim 9, this method claim comprises limitations corresponding to that of claim 1 and the same rationale of rejection is used, where applicable. And wherein the rows are referenced with read and write pointers (Kawauchi: Figure 3, item 102; Figure 3, item 103).

Regarding claim 10, the Kawauchi/Nanba/Fujimoto system teaches wherein when the write pointer is progressed and points to a message row whose distribution complete flag is set, a not free message row signal is asserted to inform the source controller.

Regarding claim 11, this method claim comprises limitations corresponding to that of claim 7 and the same rationale of rejection is used, where applicable.

Regarding claim 12, this method claim comprises limitations corresponding to that of claim 8 and the same rationale of rejection is used, where applicable.

Regarding claim 13, the Kawauchi/Nanba/Fujimoto system teaches wherein the read request is an interrupt request of the CPU (Fujimoto: col 13, lines 22-46 specifies an interrupt is sent to the processor associated with the queue so it can start reading).

10. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), in view of Nanba (US 4,665,484) and Fujimoto (US 5,418,913), and in further view of Fried et al (US 5,142,676).

Regarding claim 2, the Kawauchi/Nanba/Fujimoto system teaches wherein the write control unit comprises:

a write pointer control unit (Kawauchi: Figure 3, item 102), for storing a write address of the target message row (Kawauchi: col 4, lines 3-17), wherein after the source controller reads the write address of the target message row, said write pointer control unit sets the distribution complete flag of the target message row (Nanba: col 1, lines 17-45 specifies a test and set instruction, which uses a lock control flag on shared memory), and progresses the write address of the target message row (Kawauchi: col 4, lines 3-17 provide the write addresses are progressed sequentially), and when the source controller completes writing the message of the target message row, the write

pointer control unit sets the write complete flag of the target message row (Kawauchi: col 4, lines 46-58 specifies changing the write data attribute flag after writing data);

The Kawauchi/Nanba/Fujimoto system does not teach further comprising:

a distribution complete flag multiplexer, coupled to the write pointer control unit and the distribution complete flags of the plurality of message rows, to output a non-distributed signal according to the distribution complete flag of the message row pointed to by the write address; or

a distribution address multiplexer, coupled to the distribution complete flag multiplexer and the write pointer control unit, to alternatively output one of the write address and the no free message row signal according to the not-distributed signal.

Fried, in a similar field of endeavor, teaches:

a distribution complete flag multiplexer (Fried: Figure 2, item 62), coupled to the write pointer control unit (Fried: Figure 3, item 85; col 6, lines 24-39) and the distribution complete flags of the plurality of message rows, (Fried: Figure 2, items 58; col 5, lines 28-33) to output a not-distributed signal (Fried: NOT FOUND signal) according to the distribution complete flag of the message row pointed to by the write address (Fried: col 7, lines 37-63 specifies that if a shared memory row has been already locked, a NOT FOUND signal is used to indicate the row can't be accessed);

and a distribution address multiplexer (Fried: Figure 3, items 102, 104, 106; col 7, lines 20-36), coupled to the distribution complete flag multiplexer and the write pointer control unit, to alternatively output one of the write address and the no free message row signal according to the not-distributed signal (Fried: col 7, lines 20-63 specify that

when it is determined the segment address has not been locked, then the LOCK signal is applied to lock the segment and then the segment is written to; and when it is determined the segment address has been locked the DISALLOW signal is asserted; See also col 6, lines 24-66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Fried for managing locked memory segments with NOT FOUND and DISALLOW signals. The teachings of Fried, when implemented in the Kawauchi/Nanba/Fujimoto system, will allow one of ordinary skill in the art to identify memory segments of the queue between two processors that have been locked and disallow writing to locked segments while allowing locking and writing to unlocked segments. One of ordinary skill in the art would be motivated to utilize the teachings of Fried in the Kawauchi/Nanba/Fujimoto system in order to allow multiple processors to identify which memory segments are currently locked and which are available for locking and writing.

Regarding claim 10, this claim contains limitations found within and corresponding to claim 2 and the same rationale of rejection is applied, where applicable.

11. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), in view of Nanba (US 4,665,484) and Fujimoto (US 5,418,913), and in further view of Balmer et al (US 5,724,599).

Regarding claim 4, the Kawauchi/Nanba/Fujimoto system teaches wherein each message row comprises data the source intends to transmit to the destination (Kawauchi: abstract).

The Kawauchi/Nanba/Fujimoto system does not teach wherein the data is a command row, to store a command, and a data row, to store data.

Balmer, in a similar field of endeavor, teaches wherein the data is a command (instruction) row, to store a command, and a data row (Balmer: Figure 2, items 11, 12, 13, 14), to store data.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Balmer for splitting data into instruction rows and data rows. The teachings of Balmer, when implemented in the Kawauchi/Nanba/Fujimoto system, will allow one of ordinary skill in the art to organize data sending from one processor to the next by splitting it into instructions and data. One of ordinary skill in the art would be motivated to utilize the teachings of Balmer in the Kawauchi/Nanba/Fujimoto system in order to allow the receiving processor to easily identify which part of the message is an instruction and which part is data.

Regarding claim 5, the Kawauchi/Nanba/Fujimoto/Balmer system teaches wherein the size of the command row is four bytes (Balmer: col 10, line 52 – col 11, line 10 specify 32 bit instructions).

Regarding claim 6, the Kawauchi/Nanba/Fujimoto/Balmer system teaches wherein the size of the data row is a multiple of four bytes (Balmer: col 10, line 52 – col 11, line 10 specify data is stored in 32 bit words).

Cited Pertinent Prior Art

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Greenstein et al (US 7,724,551) discloses a shared buffer access system that uses write protect and fetch protect flags.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY NICKERSON whose telephone number is (571)270-3631. The examiner can normally be reached on M-Th, 8:30-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on 571-272-3868. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. N./
Jeffrey Nickerson
Examiner, Art Unit 2442

/Andrew Caldwell/
Supervisory Patent Examiner, Art Unit 2442